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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,365	09/04/2003	Michael Norman Day	AUS920030531US1	8448

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,365	DAY ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-14,16,18,19 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-14,16,18,19 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-21 have been presented for examination in this application. In response to the last Office Action, The specification has been amended, claims 11,15,17,20 were cancelled, claims 1-10,12-14,16,18-19,21 have been amended, claims 22-23 were added. As a result, claims 1-10,12-14,16,18-19,21-23 are now pending in this application.

Claims 1-10,12-14,16,18-19,21-23 are rejected.

Applicant's arguments filed 1/23/06 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

All rejections and objections not explicitly repeated below are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6,8-10,12-14,18-19,21 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimill et al (US 6430656) in view of Arimilli et al (US 6145057).

As in claim 1, Arimilli'656 describes a computer system (Arimilli'656 Fig 1) comprising: a plurality of memory regions each having a different address range and a corresponding class

identifier (Fig 2: #13 remaining bits, group selector; Fig 2: #16 congruence class ID; column 16 line 57 to column 7 line 34); a range register coupled to receive an address and configured to produce (Arimilli'656 Fig 2: #11 address register, column 4 lines 22-66): (i) the class identifier corresponding to the memory region having an address range that includes the received address (Arimilli'656 Fig 2: #16, column 6 lines , or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address; As for the default class identifier of the claim, Arimilli'656 column 6 lines 33-45 teaches that certain blocks' physical addresses can be absent from memory mapping and they are categorized as unused pages, Arimilli'656 column 5 line 50 to column 6 line 5 further teaches a technique for the block addresses received that in exceeding of the mapping to the associative numbers, these blocks should be mapped to the partition with the same property of unused associative bit. Thus Arimilli'656 clearly suggests of mapping these blocks into a default category/class of unused pages for caching purpose.

The claim further recites a cache comprising a plurality of sets, a replacement management table (RMT) having a plurality of entries (Arimilli'656 Fig 2: #25 column 4 lines 28-36), wherein each of the entries corresponds to one of the class identifiers and to one of the sets of the cache, and wherein the entries of the RMT are configured to store data that define the sets of the cache that may be used to store data retrieved from each of the memory regions (Arimilli'656 Fig 2: #20, #25 directory stores information about information array, column 4 lines 28-36), and wherein the RMT is coupled to receive the class identifier produced by the range register and confirmed to produce a tag replacement control indicia dependent on the received class identifier (Arimilli'656 column, and wherein the tag replacement control indicia is

indicative of the sets of the cache that may be used to store data retrieved from one of the memory regions having the received class identifier (Arimilli'656 column 4 lines 28-36 and column 6 lines 5-36 describes techniques assigning a number of associative sets in a cache to a particular congruence class or sharing among groups of congruence classes), and wherein the cache is coupled to receive data retrieved from one of the memory regions and the tag replacement control indicia, and configured to store the received data in one of the sets of the cache dependent upon the tag replacement control indicia (Arimilli'656 column 6 lines 5-36, lines 57-68 describes accessing data of the cache for both read write operations using the set associative bits and the congruence class). Although Arimilli'656 does not explicitly describes the tag replacement control indicia, Ar'057 describes a congruence cache directory that have the LRU logic and LRU indication associated with each entry of each congruence class (Ar'057 Fig 2: #40, column 3 lines 33-50). It would have been obvious to one of ordinary skill in the art at the time of invention to include the LRU logic and indication signals as suggested by Ar'057 in Arimilli'656's thereby allowing quick resolve of replacement for cache entries in response to multiple requests in a multiprocessor data processing system (Ar'057 column 1 lines 52-55; column 2 lines 9-15).

As for claims 2-4 Arimilli'656 describes wherein the class identifiers are created by software (column 7 lines 3-15, group selector supplied by instructions in a program), and wherein the class identifier creation software further comprises compiler or operating system software comprise compiler or operating system software. (claim 2; column 5 lines 30-50; column 7 lines 33-45); wherein a set of the cache is replaced based upon a least recently used

function (claim 3; column 6 lines 25-36); wherein the replacement management table uses software (claim 4; column 7 lines 34-55);

As in claim 5, the claim recites wherein class identifier creation software is employable to classify an address range as a default address range. It's rejected based on the same rationale as in the rejection of claim 1.

As in claim 6, the claim recites wherein the cache comprises a translation look-aside buffer. Arimilli'656 describes the mapping of virtual memory into physical memory (Fig 4). Thus Arimilli'656 clearly suggests using a lookaside buffer to store the translated virtual addresses to physical addresses.

As for claim 8, the claim recites a method of determining information replacement in a cache, comprising: creating a class identifier by class identifier creation software; reading the class identifier; creating a tag replacement control indicia as a function of the class identifier through employment of a replacement management table; and configuring replacement eligibility of a set in a cache as a function of the associated tag replacement control indicia. The claim rejected base on the same rationale as in the rejection of claim 1.

Claim 9 rejected based on the same rationale as in the rejection of claim 2.

Claims 10,14,19 rejected based on the same rationale as in the rejection of claim 3.

As for claims 12-13, the claim recites further comprising discarding the tag replacement control indicia if there is a hit on the cache (claim 12); the step of using the received address to retrieve corresponding data (claim 13). Arimilli'656 column 4 lines 15-28, column 5 line 65 to column 6 lines 5) clearly suggest a hierarchical cache that can obtain data from lower cache levels if data existing in lower cache levels.

Claim 17 rejected based on the same rationale as in the rejection of claim 11.

Claims 18,21 rejected based on the same rationale as in the rejection of claim 1.

Claims 16,22 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimill et al (US 6430656), Arimilli et al (US 6145057) as applied to claims 8,1 respectively and further in view of Arimilli et al (US 5974507).

As for claim 16 the claim recites employing an algorithm bit to select an algorithm for the replacement of the eligible set. The claim rejected based on the same rationale as in the rejection of claim 1. Arimilli'656 does not describe the claim's detail of algorithm bits. However, Arimilli'507 describes a cache capable to operate with different LRU algorithms by providing programmable algorithm bits (Table 1: # program bits). It would have been obvious to one of ordinary skill in the art at the time of invention to include the programmable algorithm bits as suggested by Arimilli'507 in Arimilli'656's to provide different LRU algorithms thereby allowing the cache to operate more efficiently with particular software application (Arimilli's column 5 lines 10-25; column 6 lines 14-36).

As in claim 22, the claim recites wherein the RMT is configured to store a plurality of algorithm bits each corresponding to a different one of the class identifiers, and wherein each of the algorithm bits specifies a replacement algorithm to be used to replace data in the cache for the corresponding class identifier, and wherein the tag replacement control indicia produced by the RMT is indicative of the algorithm bit corresponding to the class identifier produced by the range register. The claim rejected based on the same rationale as in the rejection of claim 16.

Claim 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimill et al (US 6430656), Arimilli et al (US 6145057), as applied to claim 1 and in view of McClure (US 5708789).

As in claim 23, the claim recites wherein the RMT is configured to store a plurality of bypass bits each corresponding to a different one of the class identifiers, and wherein each of the bypass bits is indicative of whether data retrieved from one of the memory regions having the corresponding class identifier is to be stored in the cache, and wherein the tag replacement control indicia produced by the RMT is indicative of the bypass bit corresponding to the class identifier produced by the range register. Arimilli'656 does not describe the claim's detail of bypass bits. However McClure describes a cache that have a faulty bit for each entry in the cache tag. The setting of this bit causes the microprocessor's requests to be bypassing to the main memory (McClure's column 4 lines 17-35). It would have been obvious to one of ordinary skill in the art at the time of invention to include the tag bits as suggested by McClure in Arimilli'656's thereby allowing processor requests for data in cache being bypassing and handle by main memory for example in the case the cache entry is non functional. (McClure's column 4 lines 17-33).

Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Claim 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimill et al (US 6430656), Arimilli et al (US 6145057) as applied to claim 1 and further in view of Chauvel et al (US 6826652).

As for claim 7, the claim recites wherein class identifier generation software furthercomprises a direct memory access command. Arimilli'656 does not describe the claim's

detail of direct memory access. However Chauvel describes a cache capable to be configured to operate in normal or ram-set modes whereas in ram-set mode data are filled through DMA (Chauvel's column 5 line 45 to column 6 line 10). It would have been obvious to one of ordinary skill in the art at the time of invention to include ram-set mode as suggested by Chauvel in Arimilli'656's system to preventing the cache miss for critical codes in cache (Chauvel's column 5 lines 55-60).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 3/14/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER